EXPRESS MAIL LABEL NO:

EL707909639US

ARCHITECTURE TO RELAX MEMORY PERFORMANCE REQUIREMENTS

ABSTRACT OF THE DISCLOSURE

The present invention provides a memory architecture allowing for instructions of variable length to be stored without wasted memory spaces. Instructions of one, two, and three bytes can all be retrieved in a single fetch. The exemplary embodiment divides the memory block into two ×16 memories having some special addressing circuitry. This structure logically arranges the memory into a number of rows, each of four byte-wide columns. To the first of these ×16 memories, the full address is provided. If the address is within the two columns of the second ×16 memory, the full address is also provided to the second ×16 memory. If the address is to the first of the ×16 memories, the second ×16 memory instead receives the portion of the address specifying the row with one added to it. This results in a dual row access with the last one or two bytes of 3-byte instruction being supplied by the row above the first byte. The net effect is that all the physical memory physical space is used for program code with none being wasted in the 24-bit access.